Read-only UHF Identification Device

Description
The chip is used in passive UHF read-only transponder applications. It is powered up by an RF beam transmitted by the reader, which is received and rectified to generate a supply voltage for the chip. A pre-programmed code is transmitted to the reader by varying the amount of energy that is reflected back to the reader. It implements a robust and fast anti-collision protocol. The chip is frequency independent and can be used for RF coupled applications where reading ranges in excess of 20 m and reading rates of 120 tags per second at 256 kbit/s can be attained.
The chip is backscattering data using load modulation.
Therefore the reader should be able to detect ASK and PSK modulated carrier.

Typical Applications
The chip is ideal for applications where long range, high-speed item identification is required:

- Supply chain management
- Tracking and tracing
- Access control
- Asset control
- Licensing
- Auto-tolling
- Animal tagging
- Sports event timing

Features
- Factory programmed 64 bit ID number
- High data rate: Up to 256 kbit/sFrequency independent: Typically used at 315 MHz, 433 MHz, 869 MHz, 902 - 928 MHz, 2.45 GHz
- On-chip oscillator
- On-chip rectifier
- Low voltage operation - down to 1.0 V at ambient temperature
- Low power consumption
- Low cost
- -40 to +85 °C operating temperature range

Typical Operating Configuration

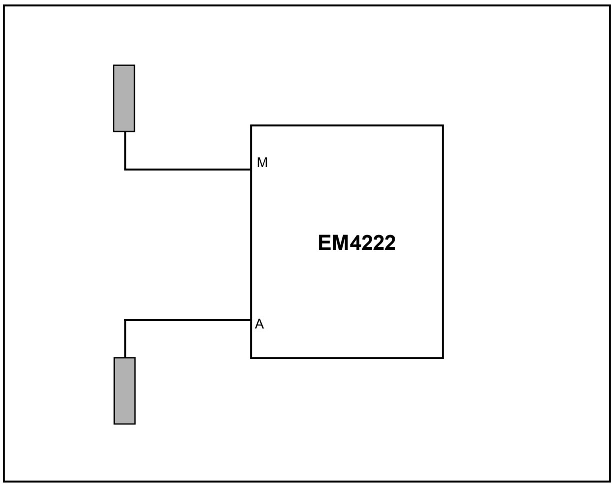


Fig. 1 Operating configuration

UHF transponders can be implemented using an EM4222 chip and an open dipole antenna.

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum DC current supplied into M	I_M (note1)	10 mA
Maximum DC voltage induced between M and V_{SS}	V_M (note1)	5 V
Storage temperature	T_{STORE}	-55 to +125°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	2000 V

note1: whichever is reached first.
V_{SS} is not accessible on the pads

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all the terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature	T_A	-40		+85	°C
DC voltage on M*	V_M			4.0	V

* The DC voltage at pad M is limited by the on-chip shunt regulator

Electrical Characteristics

V_{SUPPLY} = 2.0 V, T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
Oscillator frequency	F_{OSC}		486	512	538	kHz
Oscillator frequency	F_{OSC}	Over whole voltage range, from -40°C to +85°C	368	512	640	kHz
Power-on reset threshold	V_{PONR}	V_{SUPPLY} rising	1.3	1.4	1.5	V
Power-on reset hysteresis	V_{PHYS}			200		mV
Static current consumption	I_{STAT}	V_M = 1 V		1	5	µA
Input series impedance	Zin	869 MHz ; -10 dBm		Tbd		Ω
Input series impedance	Zin	915 MHz ; -10 dBm		Tbd		Ω
Input series impedance	Zin	2.45 GHz ; -10 dBm		Tbd		Ω

Block Diagram

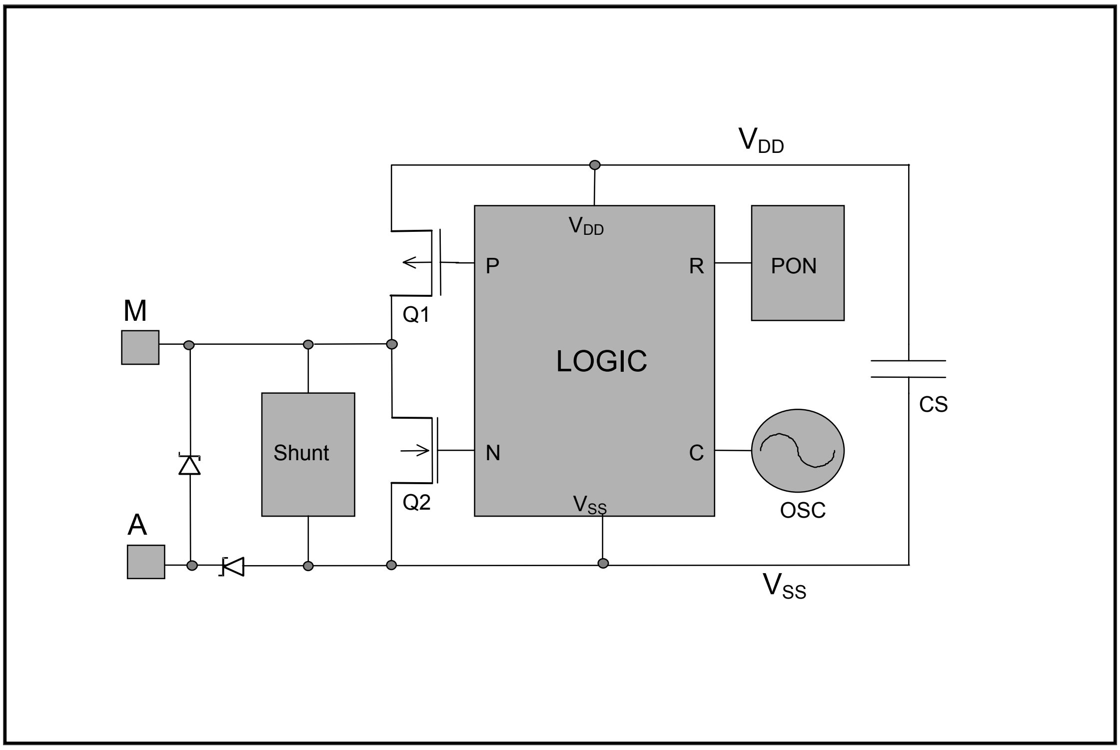


Fig. 2 Block diagram

Functional Description

Shunt regulator
The shunt regulator has two functions. It limits the voltage across the logic and protects the Schottky rectifier diodes.

Oscillator
The on-chip RC oscillator has a center frequency of 512 kHz. It supplies a clock to the logic and defines the data rate.

Power-on reset (PON)
The reset signal keeps the logic in reset when the supply voltage is lower than the threshold voltage. This prevents incorrect operation and spurious transmissions when the supply voltage is too low for the oscillator and logic to work properly. It also ensures that transistor Q2 is off and transistor Q1 is on during power-up to ensure that the chip starts up.

Modulation transistor
The N channel transistor Q2 is used to modulate the transponder antenna. When it is turned on it loads the antenna, thereby changing the load seen by the reader antenna, and effectively changing the RCS of the tag and the amount of energy that is reflected to the reader.

Charge preservation transistor
The P channel transistor Q1 is turned off whenever the modulation transistor Q2 is turned on to prevent Q2 from discharging the power storage capacitor (CS). This is done in a break-before-make manner, i.e. Q1 is first turned off before Q2 is turned on, and Q2 is turned off before Q1 is turned on.

LOGIC block
After the power-on reset has disappeared, the chip boots by reading a seed value into the random number generator. The least significant 16 bits of the ID (the CRC) is used as a seed.
The chip then enters its normal operating mode, which consists of clocking a 16 bit timer counter with the bit rate clock until it compares with the number in the random number generator. At this point a code is transmitted. The random number generator is clocked to generate a new pseudo random number, and the 16 bit counter is reset to start a new delay.
The width of the comparison between the 16 bit random number and the 16 bit delay count determines the maximum possible delay between transmissions (reading rate). Any one of four maximum delay settings can be pre-programmed.

Data encoding method
The transmitted code consists of an 11 bit preamble followed by the 64 code bits. The preamble consists of 8 start bits (ZEROES), followed by a SYNCH. The SYNCH consists of a LOW for two bit periods followed by a ONE. A ONE is represented by a HIGH in the first quarter of the bit period, while a ZERO is represented by a HIGH in the third quarter of the bit period.

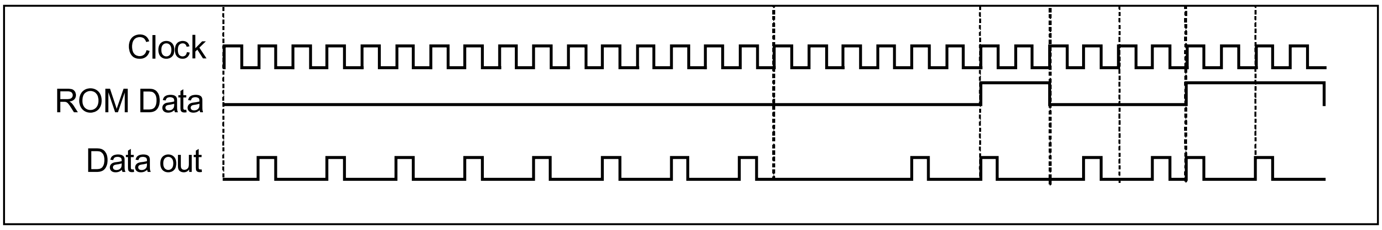


Fig. 3. Down link data encoding

ROM programming
The EM4222 contains two laser fuse ROM blocks that are pre-programmed by the foundry. The ROM blocks are split in two parts: the Code ID ROM and the Control ROM.

CODE ID ROM
This ROM contains the 64 bit ID code. The foundry will automatically program an 8 bit IC manufacturer code according to ISO/IEC 7816-6/AM1, a unique 38 bit ID and a 16 bit CRC (Refer to figures 4 and 5). The two most significant bits are reserved for future extensions. The most significant bit of the ID code is programmed into bit 0 of the ROM, which is transmitted first.

CONTROL ROM
The operational modes of the EM4222 are pre-programmed into the CONTROL ROM. Five standard versions are available as described in the chapter **Control ROM Bit definition**.

ID Code Structure

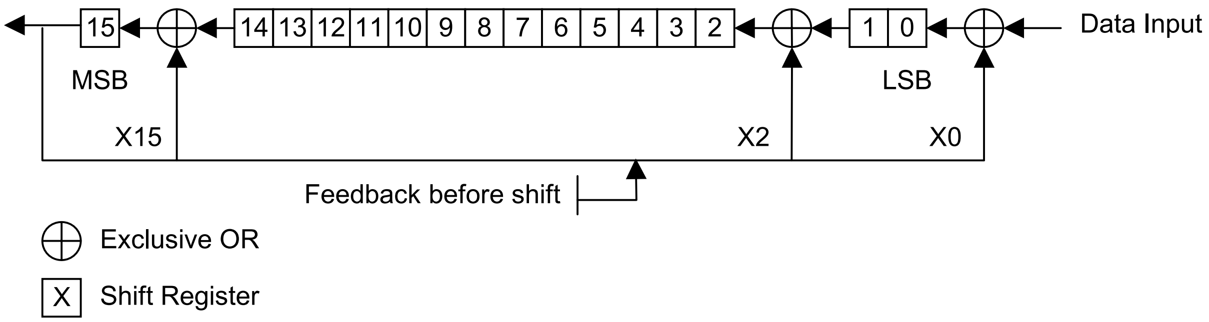
EXT	MAN	UID	CRC
Bit 63,62	Bit 61-54	Bit 53-16	Bit 15 - 0

EXT: Programmed 00 to indicate 64 bit read-only device
MAN: 8 bit IC manufacturer's code (00010110 for EM)
UID: 38 bit unique ID
CRC: 16 bit CRC
Example codes:

```
ID = 0000000000, CODE = 058000000000A4DE
ID = 0123456789, CODE = 058123456789CCDD
ID = 3FFFFFFFFF, CODE = 05BFFFFFFFFF2EDF
```

Fig. 4 ID code structure

CRC Block Diagram



CRC-16 Generating polynomial = X16 + X15 + X2 + 1. The CRC is seeded with FFFF. Transmit MSB first.

Fig. 5 CRC Block diagram

Application Overview

The EM4222 chip implements a fast and reliable anti-collision protocol. The chip is typically used in passive transponder applications, i.e. it does not require a battery power source. Instead, it is powered up by an RF beam transmitted by the reader, which is received and rectified to generate a supply voltage for the chip. A pre-programmed code is transmitted to the reader by varying the amount of energy that is reflected back to the reader. This is done by modulating an antenna, thereby effectively varying the radar cross section (RCS) seen by the reader.
A UHF tag can be implemented using an EM4222 chip and an antenna (typically printed). High reading distances (> 20 m) and high data rates (up to 256 kbit/s) can be achieved.
The basis of the anti-collision protocol is that tags transmit their own codes at random times to a reader. By just listening and recording unique codes when they are received, the reader can eventually detect every tag. The reader typically detects collisions by checking a CRC. Its main advantage is that the reader design is simple, and the spectrum requirement is low – a very narrow band is required.

Figure 6 shows a sequence of three transponders. The reader starts to read transponder 3 but during its data transmission, transponder 1 starts to transmit. In this case, due to the CRC check, the collision is detected and the transmission discarded. Next both transponders 2 and 3 are detected successfully and eventually transponder 1 as well. A transponder is registered only if it transmits a complete ID without any errors.

Max timing delay for ID transmit

All communication packets consist of 64 bit ID bits plus 11 header bits = 75 bits.

Calculation for the EM4222V2, i.e. data rate is 64 kbps, maximum random delay is 16 kbits.

Max random delay is 16 kbits / 64 kbps = 250 ms.
The initial random delay is 8 times faster on the first transmissions.
So the Max initial random delay is 32 ms.
The first transmission will occur between 16 bit clocks and the max random delay:
power-up +250µs and **power-up +32 ms**.

The *mean value* is **16 ms** for the first transmission.

Max. time to read full ID:
Max. initial Rnd delay + 75 bits @ 64 kbps

Min. delay (µs)		Max. Rnd delay (ms)		Message (ms)
		Initial	after 4 transmissions	
256	V1	62	8	1.2
256	V2	250	32	1.2
64	V3	16	2	0.3
64	V4	62	8	0.3
64	V5	250	32	0.3

Example Transmission Sequence

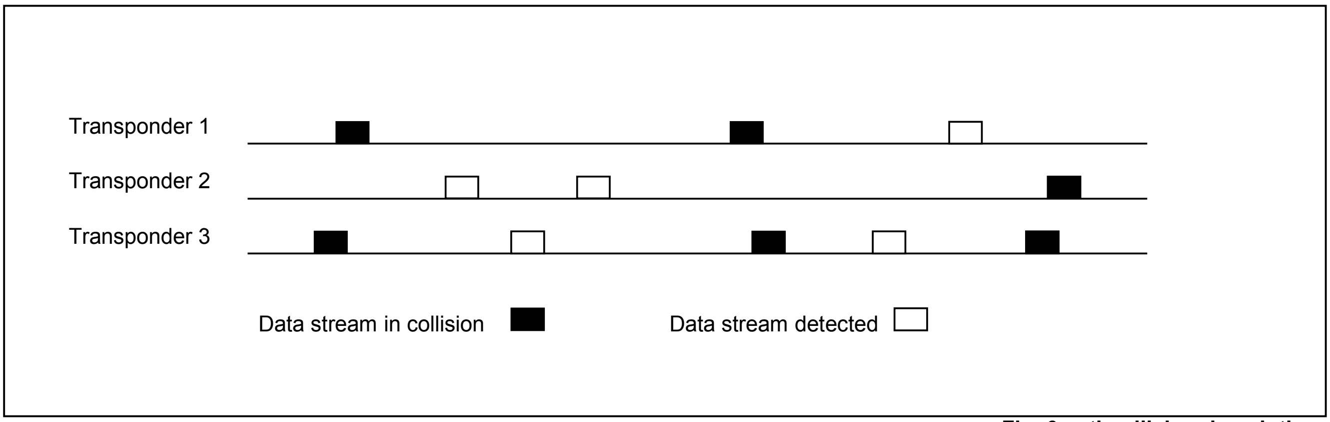


Fig. 6 anti-collision description

Protocol Saturation

As the number of tags in a reader beam is increased, the number of collisions between transmissions increases and it takes longer to read all the tags. This process is not linear. To read twice as many tags could take more than twice as long. This effect is called protocol *saturation*. The EM4222 implements a patented technique for reducing the effects of saturation.

It is also possible to optimize the protocol for various applications (few fast moving tags vs. large numbers of slow moving tags) by setting the maximum random delay between transmissions. Four different settings are available from 1 kbits to 64 kbits. A higher setting means it will take longer to read a small number of tags, but it will take a larger number of tags to saturate the channel.

Figure 7 shows average reading times for the standard versions. Maximum reading time (3σ) for a given number of tags can be up to double the average reading time. With both V4 and V5 a minimum of 60 tags can be read in one second.

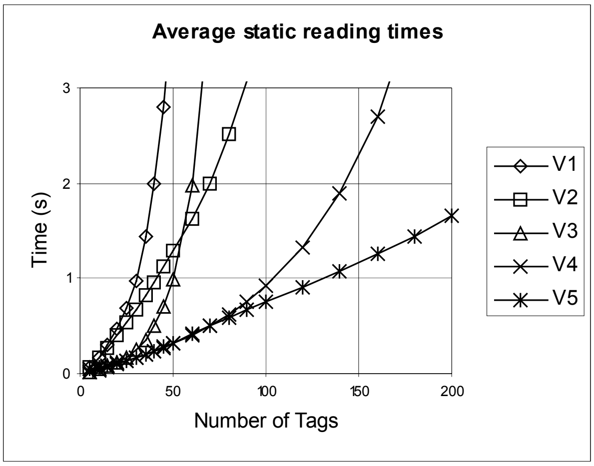


Fig. 7

Figure 8 shows average reading rate for the standard versions. V4 and V5 achieve maximum reading rates of nearly 200 tags per second.

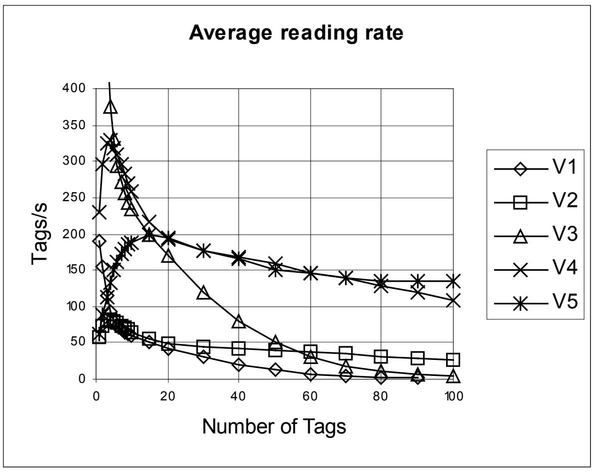


Fig. 8

Figure 9 shows maximum speeds that can be achieved with a reader that conforms to European power levels (approximately 2 meter reading range and beam width). These speeds can be more than doubled for applications in the USA.

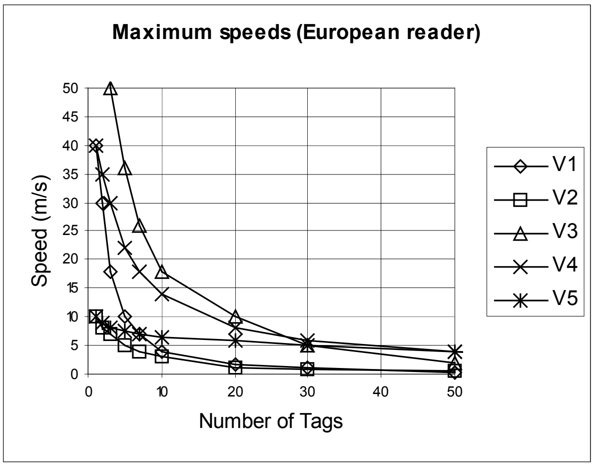


Fig. 9

V4 tags are suitable for most SCM applications. V5 tags should be used where more than 100 tags will be read simultaneously. V3 tags should be used for high-speed applications.

Control ROM Bit Definition

The operational modes are pre-programmed into the 5 bit CONTROL ROM. This operational mode is defined as the version number of the chip, as described in the table hereunder.

Part number	Tx Data rate	Max interval
EM4222V1	64kbps	4k
EM4222V2	64kbps	16k
EM4222V3	256kbps	4k
EM4222V4	256kbps	16k
EM4222V5	256kbps	64k

Chip and packaging information

Pad location

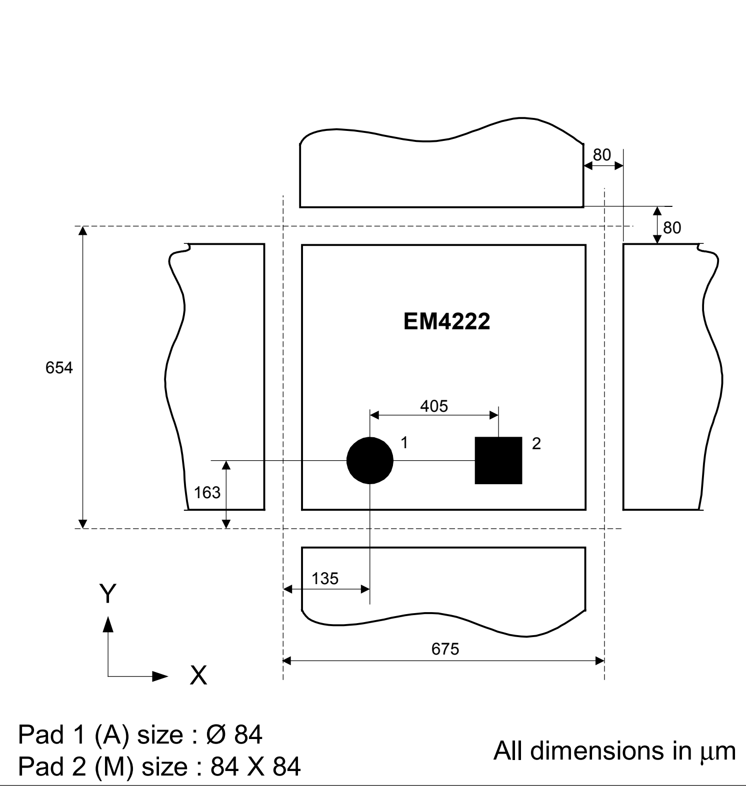


Fig. 10 Pad location diagram

Bump location

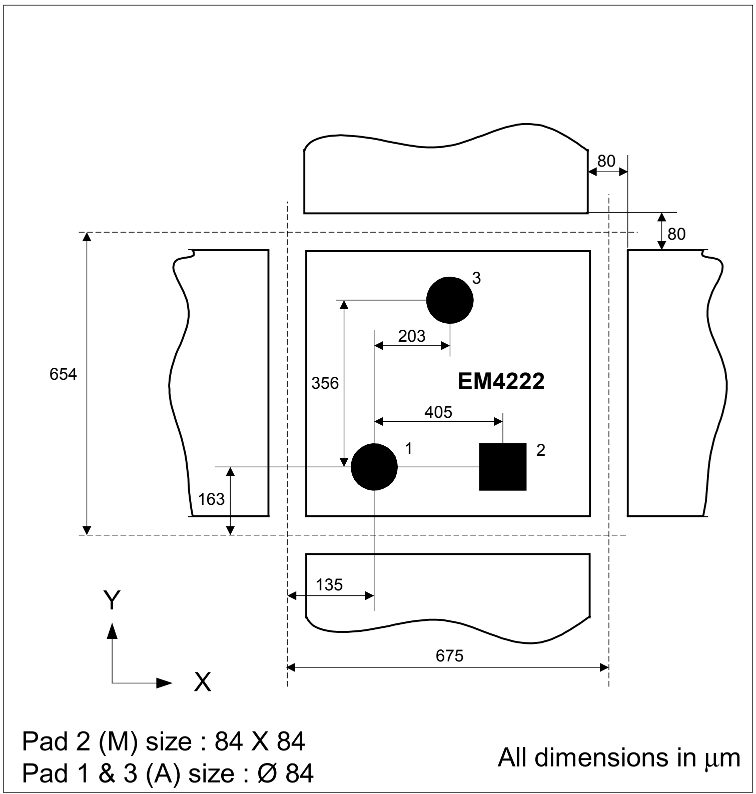
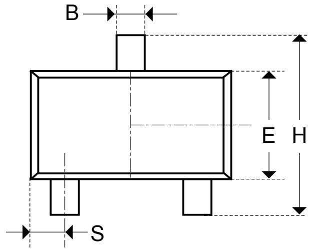


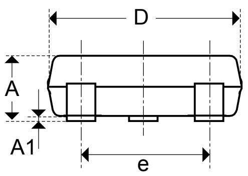
Fig. 11 Bump location diagram – Bump 3 unconnected

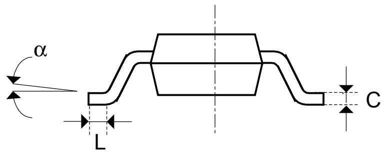
SOT 23 package outline



NOTES:

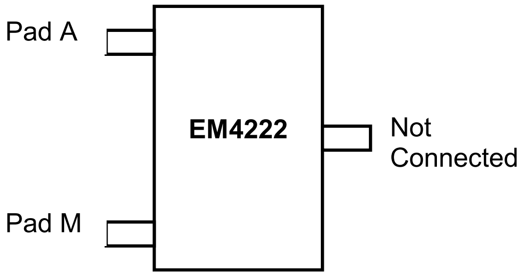
- D&E do not include mold flash
- Mold flash or protrusions not to exceed .15mm (.006")
- Controlling dimension: millimeter





Dim	Min [mm]	Max [mm]
A	0.787	1.194
A1	0.025	0.127
B	0.356	0.559
C	0.086	0.152
D	2.667	3.048
E	1.194	1.398
e	1.778	2.032
H	2.083	2.489
L	0.102	0.305
S	0.432	0.559
α	0°	8°

SOT 23 pinout



Top marking:

D	A	V	#

where # = version number (1, 2, 3, …)

Ordering Information

Please specify the complete part number when ordering (without spaces between letters).

DIE FORM:

EM4222 V1 WS 11 -

Version:
V1 = data rate:64k, interval:4k
V2 = data rate:64k, interval:16k
V3 = data rate:256k, interval:4k
V4 = data rate:256k, interval:16k
V5 = data rate:256k, interval:64k

Bumping:
" " (blank) = no bumps
E = with Gold Bumps

Thickness:
7 = 7 mils (178um)
11 = 11 mils (280um)

Die form:
WW = Wafer
WS = Sawn Wafer/Frame

PACKAGE FORM:

EM4222 V1 SP3A -

Version:
V1 = data rate:64k, interval:4k
V2 = data rate:64k, interval:16k
V3 = data rate:256k, interval:4k
V4 = data rate:256k, interval:16k
V5 = data rate:256k, interval:64k

Package/Card & Delivery Form:
SP3B = SOT-23 on tape & reel, 3000 pcs

Standard Versions:

The versions below are considered standards and should be readily available. For the other delivery form, please contact EM Microelectronic-Marin S.A. Please make sure to give the complete part number when ordering.

Part Number	Version Number	Package/Die Form	Delivery form/Bumping
EM4222V2WW11	V2	Unsawn wafer	No bumps
EM4222V2WS7	V2	Sawn wafer	Gold bumps
EM4222V2SP3A	V2	SOT-23	-
EM4222V4WW11	V4	Unsawn wafer	No bumps
EM4222V4WS7	V4	Sawn wafer	Gold bumps
EM4222V4SP3A	V4	SOT-23	-
EM4222V5WS11	V5	Sawn wafer	Gold bumps